REMARKS

Applicants hereby request reconsideration of the present application in view of the foregoing amendments and the following remarks.

Claims 1-7 are pending in the application. Claim 5 has been amended to be in independent form. Claim 1 is amended to include dependent claim 3. Marked up versions showing the changes are attached. Claim 8 has been added dependent off of claim 5. No new matter has been added.

Rejection under 35 USC §103(a)

The Examiner has rejected claims 1-4 under 35 USC § 103(a), as being unpatentable over Kang (6,052,133) in view of Nally et al (5,748,968). Applicants have considered the Examiner's remarks and have amended claim 1 to include dependent claim 3.

Applicants disagree that the teachings of three separate and concurrently operable internal buses that connect said graphical controller and a respective one of said core controller, said bus bridge and said unified memory control are rendered obvious by the teachings of single chip multi-function controller of Kang. In the cited Kang reference, graphics processor 144 is connected to (a) the host interface 142 via an **internal bus 148**; (b) the PCI bridge 264 and the host bus interface 262 via an internal bus 268, a communications link interface 260, a communications link 126, a communications link interface 140, and the **internal bus 148**; and (c) the system memory controller 146 via the **internal bus 148**. In other words, the graphics processor 144 in the system of Kang is connected to the host interface 142, the PCI bridge 264, the host bus interface 262 and the system memory controller 146 using **a single internal bus 148**.

There is no motivation cited in Kang for one skilled in the art to use three separate internal buses for connecting the graphical processor to the other devices as recited in Claim 1. Because the system of Kang only uses a single internal bus, there is also no motivation for one skilled in the art to use three separate internal buses that are configured to be concurrently operable as recited in Claim 1. Claim 5 has been

rewritten in independent form and is considered to be allowable since it was not rejected over the prior art.

Applicants respectfully submit that the foregoing amendment overcome the obviousness rejection. Accordingly, withdrawal of the rejection is solicited.

Rejection under the Doctrine of Double Patenting

The Examiner has rejected claims 1-7 under the Doctrine of Obviousness Double Patenting, as being unpatentable over claims 1-9 of co-pending application 09/199,270. Applicants respectfully request that the Examiner notify Applicants' undersigned attorney by telephone when application 09/199,270 has been allowed. Applicants will then fax a terminal disclaimer to the Examiner for this application (i.e. 09/199,478), as provided in MPEP 804, for One Way Obviousness.

CONCLUSION

In view of the foregoing remarks, Applicants urge that the present claims are in condition for allowance. An early notice in this regard is earnestly solicited. Should there be any questions regarding this application, the Examiner is invited to contact the undersigned at the telephone number shown below.

Respectfully submitted,

Date 7 June 2001 By S. A. Bent

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Should additional fees be necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge Deposit Account No. 19-0741 for any such fees; and applicant(s) hereby petition for any needed extension of time.

MARKED UP COPY OF THE CLAIMS SHOWING CHANGES MADE

1. (Amended) An integrated circuit device for use in a computer system that includes a processing unit, a host bus connected to the processing unit, an input/output bus, a peripheral device connected to the input/output bus, a monitor, and a system memory, said integrated circuit device comprising:

a core controller adapted to be connected to the host bus;

a bus bridge connected to said core controller and adapted to be connected to the input/output bus;

a graphical controller connected to said core controller and said bus bridge and adapted to be connected to the monitor; [and]

a unified memory control unit including: a graphical-memory address/data path connected to said graphical controller; a system-memory address/data path connected to said core controller; a centralized memory arbiter connected to said core controller and said graphical controller so as to detect a respective memory request signal therefrom; and a unified memory controller adapted to be connected to the system memory and connected to said graphical-memory and system-memory address/data paths, said unified memory controller being further connected to and controlled by said memory arbiter so as to be adapted to allocate access of the system memory to one of said graphical controller and said core controller via a corresponding one of said address/data paths in accordance with status of the memory request signals received by said memory arbiter[.]; and

three separate and concurrently operable internal buses that connect said graphical controller and a respective one of said core controller, said bus bridge and said unified memory control unit.

2. The integrated circuit device as claimed in Claim 1, wherein said core controller, said bus bridge, said graphical controller and said unified memory control unit are built into a single integrated circuit package.

3. (Canceled)

4. (Amended) The integrated circuit device as claimed in Claim [3] 1, wherein said internal buses run at the same clock domain as the host bus.

5. (Amended) [The integrated circuit device as claimed in Claim 1, further comprising:] An integrated circuit device for use in a computer system that includes a processing unit, a host bus connected to the processing unit, an input/output bus, a peripheral device connected to the input/output bus, a monitor, and a system memory, said integrated circuit device comprising:

a core controller adapted to be connected to the host bus;

a bus bridge connected to said core controller and adapted to be connected to the input/output bus;

a graphical controller connected to said core controller and said bus bridge and adapted to be connected to the monitor;

a unified memory control unit including: a graphical-memory address/data path connected to said graphical controller; a system-memory address/data path connected to said core controller; a centralized memory arbiter connected to said core controller and said graphical controller so as to detect a respective memory request signal therefrom; and a unified memory controller adapted to be connected to the system memory and connected to said graphical-memory and system-memory address/data paths, said unified memory controller being further connected to and controlled by said memory arbiter so as to be adapted to allocate access of the system memory to one of said graphical controller and said core controller via a corresponding one of said address/data paths in accordance with status of the memory request signals received by said memory arbiter;

a first internal bus that interfaces said core controller and said bus bridge;

a second internal bus that interfaces said graphical controller and said core controller;

a third internal bus that interfaces said graphical controller and said bus bridge;

a fourth internal bus that interfaces said graphical controller and said unified memory control unit; and

a fifth internal bus that interfaces said core controller and said unified memory control unit.

6. The integrated circuit device as claimed in Claim 5, wherein said first, second, third, fourth and fifth internal buses are separate from each other and are operable concurrently.

7. The integrated circuit device as claimed in Claim 5, wherein said first, second, third, fourth and fifth internal buses run at the same clock domain as the host bus.

8. (New) The integrated circuit device as claimed in Claim 5, wherein said core controller, said bus bridge, said graphical controller and said unified memory control unit are built into a single integrated circuit package.